REMARKS

Upon entry of this Response, claims 1, 12, 20, and 21 will be amended and claims 6-7, 15-19, and 22 will be canceled. Thus, claims 1-5, 8-14, and 20-21 will remain pending. No new matter has been added. Reconsideration of the rejections and allowance of the application are respectfully requested.

As a preliminary matter, claims 1, 12, and 20 have been amended in view of the Examiner's helpful comments and should now comply with 35 USC § 112.

The previously pending claims were rejected under 35 USC § 102 as being unpatentable over US Publication No. 2004/0148473 A1 ("Hughes").

Claim 1 as amended recites that a requesting agent processor determines that IO traffic is to be received at a target processor cache. The requesting agent processor transmits routing information to a write agent, which then directs information packets of the IO traffic to the target processor cache and status information to a requesting agent cache of the requesting agent processor.

Support for these elements can be found, for example, in FIG. 6 of the present application and the accompanying description in the specification at page 7, line 16 through page 8, line 12. In this case, the cache 612 of the first processor 610 is the requesting agent cache (to receive IO status information) and the cache 622 of the second processor 620 is the target processor cache (to receive IO packets).

Applicants respectfully suggest that Hughes does not disclose or suggest such features. For example, FIG. 4 of Hughes is directed to system that includes a single processor 122 [0036]. An IO device 160, such as an Ethernet controller, produces data [0035]. A memory controller 126 can arrange for the data to be written into a cache 124 of the processor [0037]. In no case, however, is IO status information transferred directly into a cache of a requesting agent processor as is now recited in claim 1.

Also consider, for example, FIG. 10 of Hughes. Although two processors 622, 626 with caches 624, 628 are shown, it is not disclosed that a write agent is to directly transfer IO packets into one cache while transferring IO status information about those packets directed into the other cache. Nor does Hughes disclose or suggest a cache associated with either the I/O device 640 or the directory/memory controller 636.

Since Hughes does not disclose or suggest a feature that is now recited in claim 1 (and claims 2-5 and 8-11 dependent thereon), reconsideration of the rejection and allowance of these claims are respectfully requested.

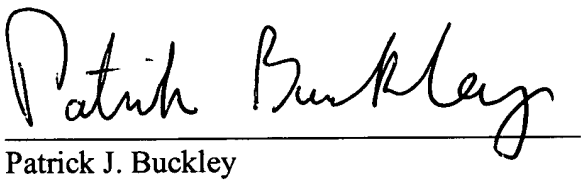
Claim 12, and claims 13-14 dependent thereon, recite limitations similar to those recited in claim 1, and are directed to an embodiment wherein the write agent is a IO controller hub. As a result, reconsideration of the rejection and allowance of these claims are respectfully requested for the same reasons.

Similarly, claim 20, and claim 21 dependent thereon, also recite limitations similar to those recited in claim 1, and are directed to an embodiment wherein the write agent is a Direct Memory Access (DMA) controller. As a result, reconsideration of the rejection and allowance of these claims are also respectfully requested.

CONCLUSION

Accordingly, Applicants respectfully request allowance of the pending claims. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned via telephone at (203) 972-0191.

Respectfully submitted,



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